## II B. Tech I Semester Supplementary Examinations, May/June - 2016 DIGITAL LOGIC DESIGN

(Com. to CSE, IT)

Time: 3 hours			Max. Marks: 70	
		Note: 1. Question Paper consists of two parts (Part-A and Part-B)  2. Answer ALL the question in Part-A  3. Answer any THREE Questions from Part-B		
		PART -A		
1.	a)	Given the two binary numbers $X = 1010100$ and $Y = 1000011$ , perform the subtraction	(3M)	
	1.	(i) X - Y and (ii) Y - X by using 2's complements.	(43.45)	
	b)	Implement the Boolean function $F = xy + x'y' + y'z$ with OR and inverter gates	(4M)	
	c)	Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to- 4-line decoder. Use block diagrams for the components.	(3M)	
	d)	Distinguish between combinational and sequential logic circuits.	(4M)	
	e)	The contents of a four-bit register are initially 0110. The register is shifted six times to the right with the serial input being 1011100. What is the content of the register after each shift and explain how?	(4M)	
	f)	Give the comparison between PROM, PLA and PAL.	(4M)	
		PART -B		
2.	a)	Perform subtraction on the given unsigned binary numbers using the 2's complement of the Subtrahend. Where the result should be negative, find its 2's complement and affix a minus sign.  (i) 10011 - 10010 (b) 100010 - 100110  (ii) 1001 - 110101 (d) 101000 - 10101	(8M)	
	b)	Convert decimal +49 and +29 to binary, using the signed-2's-complement representation and enough digits to accommodate the numbers. Then perform the binary equivalent of $(+29) + (-49)$ , $(-29) + (+49)$ , and $(-29) + (-49)$ . Convert the answers back to decimal and verify that they are correct.	(8M)	
3.	a)	Find all the prime implicates for the following Boolean functions and determine which are essential and realize the expression using simple logic gates $F(w, x, y, z) = \sum_{i=0}^{\infty} (0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$	(8M)	
	b)	Find the complement of the functions $F1 = x'yz' + x'y'z$ and $F2 = x(y'z' + yz)$ .	(8M)	
		1 of 2		