

III B. Tech I Semester Supplementary Examinations, May - 2016
LINEAR & DIGITAL IC APPLICATIONS
 (Electrical and Electronics Engineering)

Time: 3 hours

Max. Marks: 70

- Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
 2. Answering the question in **Part-A** is compulsory
 3. Answer any **THREE** Questions from **Part-B**

PART -A

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|---|--|------|
| 1 | a) Draw the circuit for level shifter. | [3M] |
| | b) List any Six characteristics of an Ideal op-amp. | [3M] |
| | c) Design a subtractor circuit using op-amp with relevant equations. | [4M] |
| | d) Define stable and quasi stable state. | [4M] |
| | e) Give the conversion time for
i) counting ADC ii) successive approximation ADC iii) dual slope ADC. | [4M] |
| | f) Draw the circuit diagram of Second order high pass filter and give its transfer function. | [4M] |

PART -B

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|---|--|-------|
| 2 | a) Draw Block diagram of Typical Op–Amp With Various Stages and explain in detail. | [8M] |
| | b) Explain the operation of differential amplifier with its transfer characteristics. | [8M] |
| 3 | a) What is the function of voltage regulator? | [3M] |
| | b) Show the standard representation of IC voltage regulator. | [3M] |
| | c) List and explain the characteristics of three terminal IC regulator. | [10M] |
| 4 | a) With the circuit diagram explain the working of Instrumentation Amplifier. | [10M] |
| | b) Design a differentiator circuit that will differentiate input signal with $f_{\max} = 100\text{Hz}$. | [8M] |
| 5 | a) Design an astable multivibrator with 50 % duty cycle using 555 timer. | [9M] |
| | b) Derive the expression for Time period of an astable multivibrator using 555 timer. | [7M] |
| 6 | a) Design and explain the operation of first order wide band pass filter with its characteristics? | [8M] |
| | b) Design and explain the operation of All Pass Filter with its characteristics? | [8M] |
| 7 | a) What is the conversion time of a 10 bit successive approximation ADC if its input clock is 5 MHz? | [8M] |
| | b) Explain the operation of D/A converter with binary weighted resistors. | [8M] |
