Code No: RT31044 **R13** SET - 1

III B. Tech I Semester Supplementary Examinations, May – 2016
DIGITAL SYSTEM DESIGN & DIGITAL IC APPLICATIONS
(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	What are the steps involved in FPGA Design Flow using VHDL.	[4M]
	b)	Define simulation and synthesis.	[4M]
	c)	Write the advantages of PLA over other simple PLDs.	[4M]
	d)	Draw the CMOS inverter circuit and Explain.	[3M]
	e)	Write VHDL code for half subtractor using data flow modeling.	[4M]
	f)	Write VHDL code for D Flip Flop with asynchronous reset using behavioral modeling.	[3M]

PART –B

2	a)	Explain the data types in VHDL.	[5M]
	b)	Write in brief about the history of VHDL.	[5M]
	c)	What are the different types of objects in VHDL? Explain.	[6M]
3	a)	What is the importance of constraints in VHDL? Explain various constraints.	[8M]
	b)	Explain Electronic Design Interchange Format netlist representation in detail.	[8M]
4	a)	Draw and explain the 1-bit memory cell of a Dynamic RAM.	[8M]
	b)	Implement a 2-bit squarer logic circuit using PROM.	[8M]
5	a)	What is the necessity of interfacing in logic circuits? Write a brief note on interfacing TTL with CMOS?	[8M]
	b)	Draw and explain the 2-input NAND gate using TTL logic.	[8M]
6	a)	Explain the operation of 8-bit barrel shifter with a neat diagram.	[8M]
	b)	Write VHDL codes which convert a fixed point number into a floating point number.	[8M]
7	a)	Write VHDL code for a 3-bit synchronous binary even counter.	[8M]
	b)	Design MOD-16 synchronous counter using T- Flip-Flop?	[8M]

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